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EXAMINER	
LEE, CHUN KUAN	

ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 04/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/727,102	BARRENSCHEEN ET AL.	
	Examiner	Art Unit	
	Chun-Kuan (Mike) Lee	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 January 2006 and 02 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

ftzm. fleming

FRITZ FLEMING
PRIMARY EXAMINER
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Supervisory 4/18/2006

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, filed on 01/27/2006, with respect to the rejections of claims 1-10, 12-14 and 18-22 under 35 U.S.C. § 103(a) has been fully considered but is not found to be persuasive.

2. Applicant's arguments with respect to claims 11 and 15-17 have been considered but are moot in view of the new ground(s) of rejection. The current amended claims 11 and 15-17 are moot because the diagnostic data are transmitted in synch (as in synchronized) with a transmitted clock signal, where as the original presented claims 11 and 15-17 stated the diagnostic data are transmitted in time (as in simultaneous or along with) with a transmitted clock signal. Rejection of claims 11 and 15-17 under 35 U.S.C. § 112 are withdrawn and claims 1-22 are currently pending for examination.

3. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., transfer of the load control data and the pilot data are transmitted over a same transmission channel) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

4. In responding to applicant's argument that the applied references do not teach or suggest a line for transmitting load control data and pilot data, wherein the load control data and the pilot data are transmitted over a same transmission channel, as stated on page 9, lines 21-27. The argument has been fully considered but is not found to be persuasive

The amended claim (amended independent claim 1) does not state that the load control data and the pilot data are transmitted over a same transmission channel, but rather the claim reiterates the limitation comprising "...transmitting the load control data and the pilot data via a second line connected between the first and second semiconductor chips", in amended claim 1, lines 12-14. Furthermore, in the Applicant Admitted Prior Art (AAPA) in Fig. 1 does show the claimed limitation as stated in the amended claim 1, wherein the transmission of the load control data (AAPA, DATA2 of Fig. 1) and the pilot data (AAPA, DATA1a of Fig. 1) via a second line connected between the first and second semiconductor chip (AAPA, Fig.1), wherein the second line is a single communication line interconnecting the first and second semiconductor chip comprising the load control data line (DATA2 line) and the pilot data line (DATA1a line). Examiner reiterates his rejection of claims 1-10, 12-14 and 18-22 under 35 U.S.C. § 103(a) and rejects claims 11 and 15-17 under 35 U.S.C. § 103(a) in detail below.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-10, 12 and 18-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arslain et al. (US Patent 6,366,153) in view of Applicant Admittance Prior Art (AAPA).

6. As per claim 1, Arslain teaches a system and a method comprising a first semiconductor chip (Fig. 1, ref. 102) and a second semiconductor chip (Fig. 1, ref. 100) connected thereto,

where the second semiconductor chip is additionally connected to an electrical load and drives the electrical load (Fig. 1, ref. 118) on the basis of a timing which is defined by load control data (a serial clock (SCLK) and a serial data (SDI)) (Fig. 1; col. 2, ll. 46-67 and col. 3, ll. 1-7),

where the first semiconductor chip transmits to the second semiconductor chip the load control data and pilot data (serial clock (SCLK), serial data (SDI), chip select (CS) of Fig. 1) which control the second semiconductor chip (Fig. 1; col. 2, ll. 63-67 and col. 3, ll. 1-7), and

where the second semiconductor chip transmits to the first semiconductor chip the diagnostic data which represent at least one of the states prevailing in the semiconductor chip and events which occurred in the second semiconductor chip (Fig. 1 and col. 3, ll. 8-50), and

AAPA expressly teaches that the transmission of the load control data (DATA2 of Fig. 1) and the pilot data (Data1a of Fig. 1) from the first semiconductor chip to the second semiconductor chip (Fig. 1); and

the second semiconductor chip includes means for transmitting the diagnostic data (DATA1b of Fig. 1) via a first line connected between the first and second semiconductor chips, and the first semiconductor chip includes means for transmitting load control data and the pilot data via a second line (communication line comprising DATA2, DATA1a of Fig. 1) connected between the first and second semiconductor chips (Fig. 1).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include AAPA's signaling of DATA1a, DATA1b and DATA2 into Arslain's system and method for controlling the gate driver.

Therefore, it would have been obvious to combine AAPA with Arslain for the benefit of providing the appropriate signaling for controlling the gate driver.

7. As per claims 2-4, please see clam 1 in view of Arslain and AAPA. Arslain further teaches that the system method further comprising:

wherein the first semiconductor chip is a processor (program controlled unit) (reference number 102, Figure 1 and column 2, lines 51-55);

wherein the second semiconductor chip is a programmable driver (power chip) (reference number 100, Figure 1);

wherein the second transmission channel further comprising:

a SCLK (transmission clock) line via which the first semiconductor chip transmits the SCLK (transmission clock) signal to the second semiconductor chip (Figure 1; column 2, lines 63-67 and column 3, lines 1-7),

a SDI (data) line via which the first semiconductor chip transmits the SDI (load control data and the pilot data) signal to the second semiconductor chip in time with the SCLK (transmission clock) signal (Figure 1; column 2, lines 63-67 and column 3, lines 1-7), and

a CS (chip select) line via which the first semiconductor chip transmits the CS (chip select) signal to the second semiconductor chip (Figure 1; column 2, lines 63-67 and column 3, lines 1-7); and

AAPA further disclose that the chip select (CS) signal signaling to the second semiconductor chip the start and end of the transmission of data intended for the second semiconductor chip via the data line ([0023], page 5).

8. As per claim 5, please see clam 1 in view of Arslain and AAPA. Arslain further teaches that the first semiconductor chip is coupled to the second semiconductor chip through a serial peripheral interface (SPI), wherein the serial interface have a plurality of

control and status registers utilized for communication between the first semiconductor chip (master) and the second semiconductor chip (slave) (column 2, lines 63-67 and column 3, lines 1-7). Therefore it would be obvious that a plurality of different control and status data are transmitted through the SDI line in units of frames in accordance with the SCLK signal, obviously using a time-division multiplexing scheme to transmit the plurality of different data (control data and pilot data).

9. As per claim 6, please see claim 5 in view of Arslain and AAPA. It is obvious that the first semiconductor chip (master), generating the SCLK signal, would define the time windows of constant length and transmit in each time window the plurality of different data (load control data frame or control data frame or no data).

10. As per claim 7, please see claim 6 in view of Arslain and AAPA. Arslain further teaches a first temperature register included within the control register of the serial interface and the first temperature register is periodically read and set by the processor (first semiconductor chip), wherein the first temperature register is used to control the PWM signal (column 3, lines 8-34). Therefore, it would be obvious that the first semiconductor chip (master) transmit load control data frame periodically, having a respective length of n time windows between the transmission and no load control data frame is transmitted during this respective length. Further more, it would also be obvious that n can be set to be $n \geq 0$ and that n is set by the processor (user of the arrangement).

11. As per claim 8, please see claim 7 in view of Arslain and AAPA. As pilot data and load control data are serially transmitted over the SDI line, it would be obvious that a pilot data frame can be transmitted only in a time window in which no load control data frame is to be transmitted.

12. As per claim 9, please see claim 6 in view of Arslain and AAPA. AAPA further disclose that the pilot data controls the transmission of the load control data ([0009], [0010], pages 2-3);

Therefore, since the pilot data and the load control data are transmitted serially over the SDI line, it would be obvious that the pilot data have a higher priority than the load control data, especially if there is a conflict for transmission between the pilot data and the load control data.

13. As per claim 10, please see clam 1 in view of Arslain and AAPA. Arslain further teaches a feedback signal from the over temperature sensing device (OTSD), transfer through the first transmission channel from the second semiconductor chip (slave) to the first semiconductor chip (master) (Figure 1 and column 3, lines 8-33). Therefore, it is obvious that the first transmission channel comprises a data line (for transmitting the feedback signal), and wherein this data line is used to transmit neither load control data nor pilot data.

14. As per claim 12, please see claim 1 in view of Arslain and AAPA. It would have been obvious that the first semiconductor chip (master) transmits appropriate feedback rate (pilot data) in order to prescribe to the second semiconductor chip (slave) what transmission rate is to be used by the second semiconductor chip (slave) to transmit the diagnostic data to the first semiconductor chip (master).

15. As per claims 18, Arslain, AAPA and Hastings teach all the limitations of claim 1 as discussed above, where AAPA further teaches the arrangement comprising:

a transmission clock line via which the first semiconductor chip (master) transmits a transmission clock signal to the second semiconductor chip (slave) (reference numbers CLK1, CLK2, Figure 1);

two data line via which the first semiconductor chip (master) transmits the load control data and the pilot data to the second semiconductor chip (slave) in time with the transmission clock signal (reference numbers DATA2, DATA1a, Figure 1); and

a chip select line via which the first semiconductor chip (master) transmits the chip select signal signaling to the second semiconductor chip (slave) the start and end of the transmission of data intended for the second semiconductor chip (slave) via the data line a first data line via which the first semiconductor chip (master) transmits the load control data and the pilot data to the second semiconductor chip (slave) in time with the transmission clock signal (reference numbers CS1, Figure 1).

Therefore, it would have been obvious for the second transmission channel to further comprise:

a first transmission clock line via which the first semiconductor chip (master) transmits a transmission clock signal to the second semiconductor chip (slave);

a second transmission clock line via which the first semiconductor chip (master) transmits the inverse transmission clock signal to the second semiconductor chip (slave),

a first data line via which the first semiconductor chip (master) transmits the load control data and the pilot data to the second semiconductor chip (slave) in time with the transmission clock signal,

a second data line via which the first semiconductor chip (master) transmits the inverse load control data and the inverse pilot data to the second semiconductor chip (slave), and

a chip select line.

16. As per claim 19, please see claim 18 in view of Arslain and AAPA. Arslain further teaches that the programmable driver is selected base on limiting electromagnetic interference (column1, lines 11-24 and column 5, lines 4-22), therefore it would be obvious that LVDS drivers or other special drivers with limited electromagnetic interference are used for the programmable (output) drivers on the first semiconductor chip (master), which output the SCLK, SDI and CS (load control data, pilot data and transmission clock) signals.

17. As per claim 20, please see claim 1 in view of Arslain and AAPA. Arslain further teaches that the first semiconductor chip (master) is couple to said single programmable driver (Figure 1), therefore it would have been obvious that the first semiconductor chip (master) is coupled to a plurality of respective different programmable (output) drivers for outputting the SCLK and SDI (load control data, pilot data and transmission clock) signals, and wherein the user of the arrangement is obviously able to set which of the plurality of different programmable (output) drivers needs to be used in each case.

18. As per claim 21, please see claim 5 in view of Arslain and AAPA. It would be obvious that the first semiconductor chip (master) is connected to a plurality of second semiconductor chips (slave), and obviously wherein a first portion of the data transmitted in a frame is intended for a first second semiconductor chip (master), and a second portion of the data transmitted in this frame is intended for a second semiconductor chip (slave).

19. Claims 11 and 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arslain et al. (US Patent 6,366,153) and AAPA, and further in view of "Data Communications Basics".

20. As per claims 11 and 17, Arslain and AAPA teach all the limitations of claim 1 as discussed above, where AAPA further teaches the arrangement comprising wherein the first line is part of a first transmission channel comprising a transmission clock line

(CLK1 of Fig. 1) via which the first semiconductor chip (master) transmits a transmission clock signal to the second semiconductor chip (slave) (Fig. 1).

Arslain and AAPA does not expressly teach the arrangement wherein the diagnostic data are transmitted in synch with a transmission clock signal generated in the second semiconductor chip and wherein this transmission clock signal is not transmitted to the first semiconductor chip; and wherein the second semiconductor chip transmits the diagnostic data in synch with the transmission clock signal received from the first semiconductor chip

"Data Communications Basics" teaches a communication system and method comprising the receiver (second semiconductor chip) receiving the transmitter's internal clock (first semiconductor chip's transmission clock signal) and the transmitter's data, the receiver then synchronizes the receiver's local oscillator to the transmitter's local oscillator, wherein said receiver's local oscillator generates the respective receiver's internal clock (second semiconductor chip's transmission clock) and the data generated by the receiver to be transmitted to the transmitter utilizes the receiver's internal clock, therefore said data generated by the receiver would be in synch with the transmitter's internal clock, wherein the receiver does not transmit the receiver's internal clock to the transmitter (first semiconductor chip) (Asynchronous vs. Synchronous Transmission Section on page 4).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Data Communications Basics' communication system and method into Arslain and AAPA's arrangement.

Therefore, it would have been obvious to combine "Data Communications Basics" with Arslain and AAPA for the benefit of providing a more robust asynchronous data transferring and receiving system and method.

21. As per claim 16, Arslain, AAPA and "Data Communications Basics" teach all the limitation of claim 11 as discussed above, where it would be obvious to oversample the diagnostic data in order for the first semiconductor chip to accurately ascertain the phase of the diagnostic data.

22. Claims 13-14 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arslain et al. (US Patent 6,366,153) and AAPA, and further in view of Hastings et al. (US Patent 6,772,251).

23. As per claim 13, Arslain and AAPA teach all the limitations of claim 12 as discussed above.

Arslain and AAPA fails specifically to teach the transmission rate is prescribed by transmitting a division factor, and wherein the second semiconductor chip (slave) divides the frequency of the SCLK (transmission clock) signal transmitted to it by the first semiconductor chip (master) by the division factor and transmits the diagnostic data to the first semiconductor chip (master) in time with the resultant signal.

Hastings teaches a system method transferring serial data between a master and a slave through a SPI, comprising of a clock divider (reference number 122, Figure 1) at

the slave for dividing down the clock frequency from the system clock line and transfer data from the slave to the master using this resulting clock frequency (Figure 1, column 1, lines 29-36, column 2, lines 60-67 and column 3,lines 1-21).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to implement the clock divider in Hastings' master and slave communication system method into Arslain's and AAPA's circuit control system method. Doing so add and further expands Arslain's and AAPA's circuit control system method by reducing the number of wires needed and increase data flow by reducing the flow of start and stop bits (Hastings, column 1, lines 29-55).

24. As per claim 14, Arslain, AAPA and Hastings teach all the limitations of claim 13 as discussed above, where AAPA further teaches the transmission clock signal supplied to the second semiconductor chip (slave) represent the transmission clock, which is used by the first semiconductor chip (master) to transmit the load control data or pilot data signal to the second semiconductor chip (slave) (reference numbers CLK1, CLK2, Data1a, Data2, Figure 1 and [0021]-[0025], page 5).

25. As per claim 22, please see claim 5 in view of Arslain and AAPA. It would be obvious that every second semiconductor chip is connected to the first semiconductor chip via a dedicated CS (chip select) line;

wherein the CS (chip select) signals are transmitted via the CS (chip select) line; and

Arslain and AAPA does not expressly teach the system and method comprising wherein the chip select signals transmitted via the chip select lines can be altered during the transmission of a frame.

Hastings further teaches an enabling (CS) signal used by the slave (reference number 304, Figure 3), wherein the enabling (CS) signal initiates the slave for transmission of data to the master and the enabling (CS) signals can be transmitted (altered) during the transmission of a frame.

Therefore, it would have been obvious to combine Hastings with Arslain and AAPA for reason stated above in claim 13.

26. Claim 15 rejected under 35 U.S.C. 103(a) as being unpatentable over Arslain et al. (US Patent 6,366,153), AAPA and "Data Communications Basics", and further in view of Hastings et al. (US Patent 6,772,251).

Arslain, AAPA and "Data Communications Basics" teach all the limitations of claim 11 as discussed above.

Arslain, AAPA and "Data Communications Basics" does not expressly teach the arrangement comprising wherein the diagnostic data are transmitted in units of frames, where a frame starts with a start bit having a prescribed value and the ends bit with one or two stop bits having prescribed value.

Hastings teaches a frame starting with a start bit having a prescribed value and ends with a stop bit having a prescribed value (Fig. 3, ref. 310, 318) for serial data transmission, therefore data would be transmitted utilizing said frame in units of frames.

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Hastings' data frame into Arslain, AAPA and Data Communications Basics' arrangement.

Therefore, it would have been obvious to combine Hastings with Arslain, AAPA and Data Communications Basics for the benefit of reducing the number of wires needed and increase data flow by reducing the flow of start and stop bits (Hastings, col. 1, ll. 29-55).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun-Kuan (Mike) Lee whose telephone number is (571) 272-0671. The examiner can normally be reached on 8AM to 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz M. Fleming can be reached on (571) 272-4145. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

C.K.L
04/10/2006

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4/12/2006